DIGITAL SYSTEM DESIGN (THEORY) EE-319

Pre-requisite: Digital Logic Design
Credit Hours 03
Contact Hours 48

RECOMMENDED BOOKS

- Verilog HDL- A Guide to Digital Design & Synthesis by Sameer Palnitkar
- Digital Design of Signal Processing Systems by Shoab Ahmed Khan

REFERENCE BOOKS

Advanced Digital Design with the Verilog HDL, M.D. Ciletti

OBJECTIVE OF COURSE

The objective of this course is to introduce the students with digital design techniques for mapping algorithms to Field Programmable Gate Arrays (FPGA). Introducing Verilog Hardware Descriptive Language (HDL) for modeling digital systems and Mentor Graphics ModelSim tool for simulation of digital systems. This course will focus on efficient implementation of Data path and Control unit using Finite State Machine for designing digital systems.

S.NO	CLO/PLOs MAPPING	DOMAIN	PLO
01	**Development** of digital design using Verilog HDL and its functional verification	**C5**	**03**
02	**Applying** simulated and synthesized digital designs using software tools such as ModelSim and Xilinx ISE	**C3**	**05**
03	**Designing** control units of digital systems using Finite State Machine (FSM) and its implement in Verilog	**C5**	**03**
04	**Designing** efficient Data path for digital system	**C5**	**03**
05	**Evaluate** and Optimize design in terms of area, throughput and timing by determining critical-paths while implementation of digital designs	**C6**	**04**

COURSE CONTENTS

Introduction to FPGAs

- Digital Systems: Implementation Spectrum
- FPGAs, Microcontrollers & ASICS
- Programmable Logic Devices
- FPGA Architecture: Configurable logic blocks, IO Blocks, Programmable interconnects
- Digital Systems application

Overview of Verilog HDL

- Verilog Syntax, Data types, Operators
- Gate Level Modeling
- Data Flow Modeling
- Behavioral Modeling
- Blocking & non-Blocking statements
- Writing Simulation Modules/ Test bench
- Coding guidelines

Digital Logic Design using Verilog HDL

- Combinational logic using Gate Level Modeling
- Combinational logic using Data Flow Modeling
- Combinational & Sequential logic using Behavioral Modeling
- Port rules for Behavioral Modeling
- Examples: Half adder, Full Adder, MUX, De-MUX, Encoders, Decoders, Comparators,
- Avoiding unwanted latches in the design
- Designing Sequential Circuits (Latch, D-Latch, D-Flip Flop, Registers)
- Block RAM, Distributed RAM, Shift Registers, Linear Feedback Shift Registers (LFSR)

Designing Control Units

- Mealy and Moore Machine Finite State Machines (FSM)
- Data path and Control units
- Designing Control units
- State Encoding Schemes
- Sequence detectors, BCD to Excess-3 conversion, Traffic Signal Controller, Ethernet loopback controller

Number's representation and Arithmetic

- Signed & Unsigned numbers, Two's complement representation
- Floating point numbers, format and arithmetic
- IEEE floating point conversions
- Floating point Vs. Fixed Point hardware
- Fixed point numbers & arithmetic, Qn.m format
- Numbers range and precision
- Qn.m addition and four types of Multiplications (signed by signed, signed by unsigned, unsigned by signed and unsigned by unsigned)

Hardware optimization

- Throughput, Latency and Timing of architecture
- Pipelining the architecture
- Critical paths in the design

Design Examples

- Digital Filters
- Implementation of FIR filter
- Implementation of IIR filter